Sun™ SPOT
Main Board Technical Datasheet
Rev 8.0

Revision 8 manufactured after October 2010

Sun Labs
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Oracle America, Inc.
16 Network Circle
Menlo Park, CA 94025
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The Basestation and Free Range SPOT

Features

- 400 MHz ARM 926ej-S Processor AT91SAM9G20
- 8Mbytes Flash Memory (4M x 16)
- 1Mbytes SRAM Memory (512K x 16)
- 802.15.4 Radio Transceiver (CC2420)
- USB 2.0 Full Speed
- 770mAhr Li-Ion Rechargeable Battery

Description

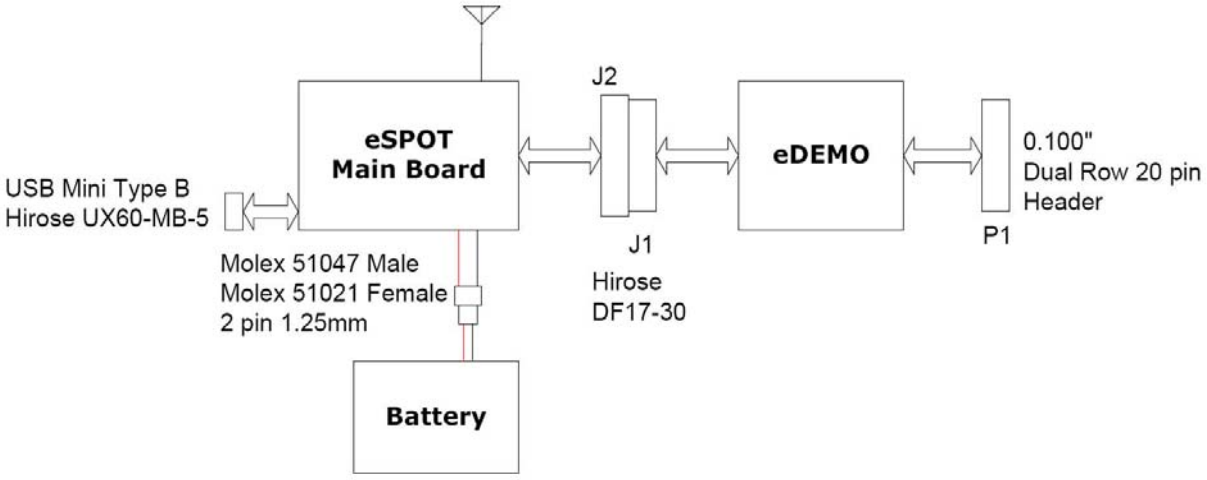
The Sun SPOT platform is the main processor board, eSPOT, running the Java “Squawk” VM and is an IEEE 802.15.4 wireless network node. An application board can be attached to the eSPOT main board

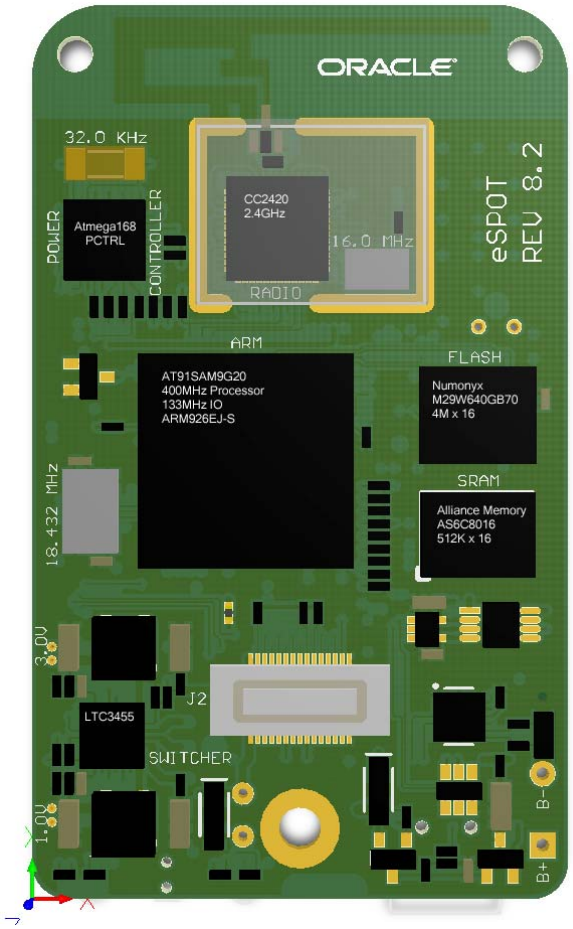
The eSPOT has flexible power management and can draw from the rechargeable battery or the USB host, or be externally powered.

The Sun SPOT is designed to be a flexible development platform, capable of hosting widely differing application modules. The Sun SPOT development kit, as supplied, contains two different configurations. One of the configurations includes a demonstration application module, the eDemo board.

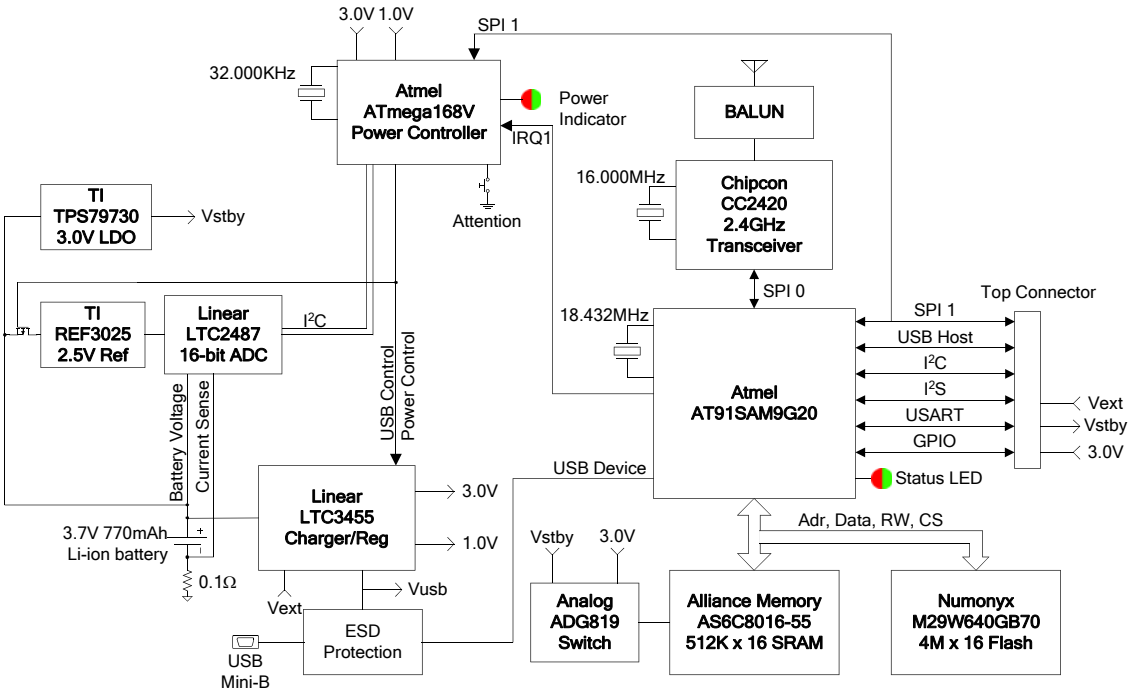
The configurations supplied in the kit are:

- Basestation SPOT - The basestation has an eSPOT main board without a battery or an application board. Power is supplied by a USB connection to a host workstation. The basestation serves as a radio gateway between other Sun SPOTs (and theoretically other 802.15.4 devices) and the host workstation.
- Free Range SPOT - This unit contains the main board with a rechargeable LI-ION prismatic battery and an example of an eSPOT daughterboard, the eDEMO board.


eSPOT
Main Board
J2
eDEMO
0.100"
Dual Row 20 pin
Header
P1
USB Mini Type B
Hirose UX60-MB-5
Molex 51047 Male
Molex 51021 Female
2 pin 1.25mm
J1
Hirose
DF17-30
Battery


ORACLE
32.0 KHz
POWER
Atmega168
PCTRL
CONTROLLER
CC2420
2.4GHz
16.0 MHz
RADIO
eSPOT
REV 8.2
ARM
AT91SAM9G20
400MHz Processor
133MHz IO
ARM926EJ-S
FLASH
Numonyx
M29W640GB70
4M x 16
SRAM
Alliance Memory
AS6C8016
512K x 16
18.432 MHz
3.0V
J2
LTC3455
SWITCHER
1.0V
B-
B+

Block Diagram



Signal Description

J2 Hirose DF17 Receptacle

Pin	Signal Name	Signal Type	Description
1,2	V_EXT	Power	+5V +/-5% at 500mA input power to the SPOT
3	USB_HOST_P	Bidirectional	USB Host Data Differential – Positive
4	MISO1	Input	SPI MISO (Master In Slave Out) data Channel 1
5	USB_HOST_N	Bidirectional	USB Host Data Differential – Negative
6	SCLK1	Output	SPI SCLK (Clock) Channel 1
7	I2C_CLK	Output	I2C SCK (Clock)
8	MOSI1	Output	SPI MOSI (Master Out Slave In) data Channel 1
9	I2C_DATA	Bidirectional	I2C SDA (Data)
10	EXT_INn	Input	External Interrupt (Active low)
11	VSTBY	Power	+3V at 35ma output power from the SPOT (always on)
12	CS_A0	Output	SPI Address A0. Address range 0 to 7. Must be stable

Pin	Signal Name	Signal Type	Description
			prior to BD_SELx.
13	P13	Multifunction	Can be programmed as GPIO (PB4), UART (TXD0) or Ethernet (EMDIO).
14	CS_A1	Output	SPI Address A1. Address range 0 to 7. Must be stable prior to BD_SELx.
15	P15	Multifunction	Can be programmed as GPIO (PB5), UART (RXD0).
16	CS_A2	Output	SPI Address A2. Address range 0 to 7. Must be stable prior to BD_SELx.
17	VCC	Power	+3V at 400mA output power from the SPOT (on when running, pulled to 0V during deep sleep)
18	BD_SEL1n	Output	SPI board select 1 active low.
19	P19	Multifunction	Can be programmed as GPIO (PB30), UART (PCK0), Ethernet (EMDC or SSC (PCK0).
20	BD_SEL2n	Output	SPI board select 2 active low.
21	P21	Multifunction	Can be programmed as GPIO (PA18), UART (TXD2), Ethernet (ERXER) or Timer (TCLK0)
22	P22	Multifunction	Can be programmed as GPIO (PA19), UART (SCK0), Ethernet (ETXCK), Timer (TIOA0) or SSC (TF0)
23	P23	Multifunction	Can be programmed as GPIO (PA15), UART (RXD2), Ethernet (ERX1), SD Card (MCCK) or SSC (RF0)
24	P24	Multifunction	Can be programmed as GPIO (PA16), UART (SCK2), Ethernet (ETXEN), SD Card (MCCDA), Timer (TIOB0) or SSC (TK0)
25	P25	Multifunction	Can be programmed as GPIO (PA14), UART (TXD3), Ethernet (ERX0), SD Card (MCDA3) or SSC (RK0)
26	P26	Multifunction	Can be programmed as GPIO (PA12), UART (SCK3), Ethernet (ETX0), SD Card (MCDA0) or SSC (TD0)
27	P27	Multifunction	Can be programmed as GPIO (PA17), UART (RXD3), Ethernet (ERXDV) or SC Card (MCDA2)
28	P28	Multifunction	Can be programmed as GPIO (PA13), UART (PCK1), Ethernet (ETX1), SC Card (MCDA1) or SSC (RD0)
29,30	GND	Power	Ground Return

Pin numbers are for the Hirose DF17 interboard connector on the SPOT main board and connects to an application board like the eDEMO. The pin numbering for the signals is mirrored from the main board to the bottom mating connector of the application board.

Theory of Operation

The eSPOT main board is host to a 32bit 400MHz ARM9 processor running a Java VM, 2.4GHz network radio transceiver and power management circuitry. The PC board measures 1.5" wide and 2.5" high. It is an eight layer 47mil thick FR4 board built to RoHS-6 compliance. It contains 244 components, 91 on top and 153 on bottom.

Main Processor

The main processor is the Atmel AT91SAM9G20 in a 247 pin fine pitch ball grid array. The processor is an ARM926ej-s and its package is 10mm x 10mm with 0.5mm ball pitch. The ARM9 processor core voltage is 1V and I/O voltage is 3V. It has 64K internal ROM which is not used and two internal 16K SRAM that are used. Peripherals actively used are USB 2.0 device, dual USART, three timer/counters, dual SPI interface, TWI (I2C) interface, JTAG TAP controller and external bus interface (EBI). The 133MHz EBI connects over a 16 bit data bus to an 8 megabyte Flash memory (4M x 16) and a 1 megabyte SRAM (512K x 16). The Ethernet MAC, USB 2.0 host, 10 bit ADC (3 channels) and SD/MMC interface are connected but not used. The SDRAM controller, image sensor controller, and watchdog timer are not used nor are all GPIO, ADC, or UART pins used. Two GPIO lines control a user-definable bi-color LED nearest to the USB connector. Green LED is controlled by Port A bit 27 (PA27) and Red LED is controlled by Port C bit 7 (PC7). Power is removed from the ARM9 during deep sleep and does not use the battery back up/real time clock portion of the internal power management module.

The 8Mbyte Flash memory is Numonyx M29W640GB70 organized as 4M x 16 bits with 70nsec access time and 30nsec page access time (4 word pages). It is in a 6mm x 8mm 48 pin fine pitch ball grid array package. It is powered with 3V and shut down during deep sleep mode. The first 64KBytes are write protected externally from the power controller. There are 128 bytes of customer lockable extended block (one time writable) which is programmed with the 64-bit IEEE extended unique identifier by the factory. The IEEE EUI is read-only and is a concatenation of a 24-bit company code (OUI) with a 40-bit extension unique for each SPOT.

The 1Mbyte SRAM is an Alliance Memory AS6C8016 with 55nsec access time. The SRAM is in 6mm x 8mm 48 pin fine pitch ball grid array package. It is powered by 3V at all times and will retain all memory contents during deep sleep.

The basic memory map for the ARM9 is :

Start	End	Description
0x00200000	0x00203FFF	16Kbyte Internal SRAM1
0x00300000	0x00303FFF	16Kbyte Internal SRAM2
0x10000000	0x107FFFFF	8Mbyte External Flash (CS0)
0x20000000	0x200FFFFF	1Mbyte External SRAM (CS1)
0xF0000000	0xFFFFFFFF	Internal Peripheral IO

Power Circuitry

The SPOT can be powered by a rechargeable battery, USB power or externally connected 5V supply. USB power and/or externally connected power can charge the battery and run the rest of the SPOT. Most of the circuitry can be shut down for long periods of time to preserve battery (deep sleep). During deep sleep, the SRAM is kept powered to retain state so the SPOT can be woken up quickly and resume where the program left off.

The SPOT uses a Linear Technology LTC3455 integrated battery charger and dual switcher in a 4mm x 4mm 24 pin quad flat package(QFN). The current mode step down switchers run internally at 1.5MHz and output 3.0V at 500mA max current (USBHP enabled) and the 1V core voltage at 200mA max current. The 3V switching regulator is similar to the LTC3406 switcher and the 1V core voltage switcher similar to the LTC3405 switcher. The 3V switcher can be turned off with the ON2 signal and the 1V switcher can be turned off using an external MOSFET connected to the switcher 1 feedback line through a 43.2K resistor and Vstby. The SPOT can go into deep sleep shutting off the switchers while still powered through USB to charge the battery.

A low quiescent current (1.2uA) low dropout regulator (LDO), TI TPS79730 regulates the battery voltage to 3V for the always-on standby power, Vstby. An Analog Devices ADG819 SPDT solid state SPDT switch switches between the high current 3V switcher during run time and the 3V low current standby power from the LDO during deep sleep. The LDO has a power good line which goes low if the output voltage drops below 2.7V. Power good deasserted will hold the power controller in reset to prevent it from malfunctioning at low voltages.

The SPOT battery is an external prismatic lithium-ion Sanyo LP523436D battery with 770mAh capacity and a nominal voltage output of 3.7V. It measures 38.5mm wide x 41.5mm high and 6.9mm thick. The battery is equipped with a Nexcon RPOPJ800 protection circuit and protects for over voltage (4.275V), over current (3A), and under voltage (2.3V). The battery connects through a Molex 51021-0200 two pin inline connector to a pigtail. The battery positive terminal is the red wire and negative terminal is the black wire. The black wire is not ground rather passes through a low side current sense resistor to ground. The mating battery connector is Molex 51047-0200.

The power is managed by the power controller, an 8-bit 8MHz Atmel ATmega168 microcomputer powered by 3V standby voltage (Vstby). The power controller has a 32KHz crystal for real time clock providing date and time at millisecond accuracy (64bit Java millisecond time). The power controller communicates with the ARM9 over a SPI interface, SPI1 which is shared with the external SPI connection. This SPI interface is buffered by 74LVC3G34 which isolates the ARM9 from the active circuitry during deep sleep. The interrupt button connects to the power controller and is used to shutdown, wake-up and interrupt the ARM9. A bicolor LED (red/green) indicates power state of the ARM9. The power controller internal analog to digital converter (ADC) monitors switcher voltages, external voltage and USB voltage. It indicates a fault condition if they are more than 5% out of range.

A Linear Technology LTC2487, an external 16-bit 4 channel ADC, is used to monitor battery voltage, current and ambient temperature. The ADC has a TI REF3025 as an external 2.5V reference with 0.2% accuracy. The reference and battery voltage divider can be switched off

(REF_EN) by the power controller to minimize current. The LTC2487 interfaces to the power controller over I2C (TWI) and sleeps when I2C is inactive. The ADC uses a low side current sense resistor to measure the current into and out of the battery. The power controller monitors the health and state of the battery using this ADC. The battery ADC is read every 200ms cycling between current, voltage and temperature measurements. Voltage and temperature measurements are taken every 1.6 seconds and current measurements taken for all other 200ms intervals.

The power controller sets the USB suspend (USB_ENn) and USB high power (USBHP) on the LTC3455 through instructions from the ARM9.

The power controller must sequence power for the ARM9 on wake-up and shutdown. During deep sleep state, the power controller goes to sleep except for the real time clock counter. It is waken up by external interrupts like the pushbutton and every 256 milliseconds for updating the real time clock. On wake-up, the power controller temporarily delays external interrupts, turns on the switchers and watches 3V switcher (VCC) to become stable. Once VCC is stable, it enables back up voltage to the ARM9 and that causes the ARM9 to issue a power on internal reset. The external reset on the ARM9 is not used. Once power is stable and the internal ARM9 reset is active, the power controller enables its own SPI channel and external interrupts.

On power off, the power controller notifies the ARM and waits a period of time so it can tear down any peripheral before shutting down. The tear-down time can be extended up to 32 seconds or terminated immediately. There is no tear-down for deep sleep. After tear-down, the backup voltage and switchers are shut off, and signals which might cause sneak paths, like FIQ, are shut down.

The power controller manages a 32bit watchdog counter with 256ms ticks. The watchdog can be set between 256ms and about 34 years. If the watchdog is not reset at a regular interval from the ARM9, it will shutdown the ARM9, wait 150ms and restart it as a cold boot. The power controller does self test and fault analysis. While running, it continually scans voltage and current for out of range values.

Symbol	Target	Error states
V_{CC}	3.0V ±10%	< 2.7V or > 3.3V power fault
V_{core}	1.8V ±10%	< 1.62V or > 1.98V power fault
V_{usb}	5.0V ±10%	< 4.5V or > 5.5V power fault
V_{ext}	5.0V ±10%	< 4.5V or > 5.5V power fault
$I_{discharge}$	< 500ma	> 500ma power fault
V_{batt}	> 3.25V	< 3.25V indicates low battery
V_{batt}	> 3.05V	< 3.05V indicates dead battery
I_{charge}	< 5ma	> 5ma indicates charging

Network Radio

The wireless network communications uses an integrated radio transceiver, the TI CC2420 (formerly ChipCon). The CC2420 is IEEE 802.15.4 compliant and operates in the 2.4GHz to 2.4835GHz ISM unlicensed bands. Regulations for these bands are covered by FCC CFR47 part 15 (USA), ETSI EN 300 328 and EN 300 440 class 2 device (Europe) and ARIB STD-T66 (Japan). Please check with country statutes for appropriate operation.

The IC contains a 2.4GHz RF transmitter/receiver with digital direct sequence spread spectrum (DSSS) baseband modem with MAC support. Other features include separate TX and RX 128 byte FIFOs, AES encryption (currently not supported), received signal strength indication (RSSI) with 100dB sensitivity and transmit output power setting from -24dBm to 0dBm. Effective bit rate is 250kbps and chip rate is 2000kChips/s. Receive sensitivity is -90dBm.

The digital control and data communications with the CC2420 use PIO port bits and the SPI channel. The CC2420 is a slave SPI bidirectional device addressed when RF_CS (PCS2) is asserted active low. PIO ports reset the CC2420 (RF_RST), power it down (RF_PWDOWN), or check the status of the receive FIFO (FIFO and FIFOP), clear channel assessment (CCA) and start of frame (SFD).

There are 33 configuration and status registers, 15 command registers and two 8-bit registers for the separate transmit and receive FIFOs. The first byte sent to the CC2420 is the address made up of 6-bit address, RAM/Register select (Bit 7) and Read/Write select (Bit 6). Following bytes are data read from or written to the CC2420.

The CC2420 is housed in a 7mm x 7mm 48pin quad leadless package (QLP or QFN). It is powered with +3.0V V_{CC} supply. The CC2420 has an internal 1.8V low drop out regulator for powering the internal RF and analog circuitry. It consumes 20ma during receive operation and 18ma for 0dBm transmit. The frequency generation uses an accurate 16MHz crystal with ±10ppm accuracy, ±10ppm stability and ±1ppm aging. The entire RF section is enclosed in an upper and lower RF shield and has modular FCC approval.

802.15.4 channel assignments are shown in the tables below.

Channel	Center Frequency
11	2405MHz
12	2410MHz
13	2415MHz
14	2420MHz
15	2425MHz
16	2430MHz
17	2435MHz
18	2440MHz

Channel	Center Frequency
19	2445MHz
20	2450MHz
21	2455MHz
22	2460MHz
23	2465MHz
24	2470MHz
25	2475MHz
26	2480MHz

The output power can be adjusted by the PA_LEVEL register, a 6 bit field.

PA_Level and output power are shown in the tables below.

PA_LEVEL	Output Power
31	0dBm
27	-1dBm
23	-3dBm
19	-5dBm

PA_LEVEL	Output Power
15	-7dBm
11	-10dBm
7	-15dBm
3	-25dBm

For more information, see the CC2420 data sheet on the www.ti.com (RF/IF Components)
The 802.15.4 standard can be retrieved from standards.ieee.org.

Antenna

The antenna is an inverted-F antenna printed on the top layer of the printed circuit board. It is tuned to 2450MHz and has a characteristic input impedance of 115Ω unbalanced. This is a folded monopole 1/4 wave with reasonable omnidirectional radiation. The antenna is matched to the balanced RF output of the CC2420 using a lumped-LC network. The RF output is also biased by the TXRX_SWITCH output of the CC2420 through a RF blocking filter.

The antenna section of the eSPOT should be kept away from all metal objects. If mounted on a motherboard, there should be no PCB traces or power planes under or around the antenna section. If possible, the eSPOT should be mounted so that the antenna is located on the edge of the board.

The FCC certification does not allow an external antenna to be connected to the eSPOT.

Mechanical

eSPOT main board 1.50” wide x 2.50” length x 0.325” depth
eSPOT basestation 1.67” wide x 2.80” length x 0.71” depth
eSPOT freerange 1.67” wide x 2.80” length x 0.92” depth
eSPOT basestation weight: 30g
eSPOT freerange weight: 62g

Operating Characteristics

Absolute Maximum Ratings

Operating Temperature with battery charging 0°C to 45°C
Operating Temperature with battery discharging -20°C to 60°C
Operating Temperature without battery -20°C to +75°C
Storage Temperature with battery -20°C to +35°C
Storage Temperature without battery -40°C to +85°C
eSPOT DC Current per I/O pin 8.0ma
Maximum External/USB voltage 6.0V

DC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
V_{ext}	External Voltage		4.5	5.0	5.5	V
V_{batt}	Battery Voltage		3.1	3.7	4.2	V
V_{usb}	USB Voltage		4.5	5.0	5.5	V
I_{usb}	USB Current Limit	V_{usb} = 5.0V, USBHP = '1' V_{usb} = 5.0V, USBHP = '0	440 60	475 80	500 100	mA mA
I_{ext}	External Current	V_{ext} = 5.0V, no eDemo V_{ext} = 5.0V, with eDemo			300 500	mA mA
I_{batt}	Battery Current - no attached board	Deep Sleep Idle Normal	55 20	65 TBD 50	75 144	µA mA mA
I_{charge}	Charge Current	V_{usb} = 5.0V, USBHP = '1' V_{usb} = 5.0V, USBHP = '0' V_{ext} = 5.0V	 425	400 50 500	470 90 575	mA mA mA
V_{low_batt}	Low battery indication				3.25	V
I_{stby_max}	Externally available standby current	J2-11 V_{stby} = 3.0V			25	mA
I_{CC}	Attached board current	V_{CC} = 3.0V			380	mA
V_{OL}	Output low level voltage	I_{OL}= 0 to 8ma	0.2	0.3	0.4	V
V_{OH}	Output high level voltage	I_{OH}= 0 to 8ma	2.6	2.7	2.8	V

Symbol	Description	Condition	Min	Typ	Max	Units
V_{IL}	Input low level voltage		-0.3		0.8	V
V_{IH}	Input high level voltage		2.0		2.7	V

AC Characteristics

Module	Min	Nom	Max	Units
SPI0		1000		Kbps
SPI1 to LED Controller		500		Kbps
SPI1 to external/power controller		263		Kbps
TWI		100		Kbps
USART	127	115200	8332800	Baud
Flash Memory (t_{cycle})		75		nsec
SRAM (t_{cycle})		60		nsec
USB		4.09		Mbps

The AC characteristics are measured values from the SPOT running default software. For specific AC characteristics, please consult the individual component datasheets.

BATTERY WARNING

Do not short-circuit battery. A short-circuit may cause fire, explosion, and/or severe damage to the battery.

Do not drop, hit or otherwise abuse the battery as this may result in the exposure of the cell contents, which are corrosive.

Do not expose the battery to moisture or rain. Keep battery away from fire or other sources of extreme heat. Do not incinerate.

Exposure of battery to extreme heat may result in an explosion.

No other battery substitutions or different chemistry batteries should be used.

Do not bypass the battery protection circuit.

Dispose of batteries properly. Do NOT throw these batteries in the trash. Recycle your batteries, if possible.

Federal Communications Commission Compliance

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures: Reorient or locate the receiving antenna. Increase the separation between the equipment and receiver. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. Consult the dealer or an experienced radio/TV technician for help.

The Sun SPOTs are supplied with a shielded USB cable. Operation with a nonshielded cable could cause the Sun SPOTs to not be in compliance with the FCC approval for this equipment. The antenna used with this transmitter must not be colocated or operated in conjunction with any other antenna or transmitter; to do so could cause the Sun SPOTs to not be in compliance with the FCC approval for this equipment. Any modifications to the Sun SPOTs themselves, unless expressly approved, could void your authority to operate this equipment.

FCC Declaration of Compliance:
Responsible Party: Oracle America, Inc., 500 Oracle Parkway, Redwood Shores, CA 94065; Phone: US +1.650.506.7000; International +1.650.506.7000
FCC IDENTIFIER: UDM3011
This device complies with Part 15 of the FCC Rules. Operation is subject to the following conditions: this device may not cause harmful interference and this device must accept any interference received, including interference that may cause undesired operation.

This device can be used as is (stand-alone) or as a module (part of a final host product). If the device will be used a module these rules must be followed:
Caution: Exposure to Radio Frequency Radiation.
To comply with FCC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons. This device must not be co-located or operating in conjunction with any other antenna or transmitter.
Module 3011 and antenna tested with must be integrated in the end product in such a way that the end user cannot access the either the module, cables or antennas.
The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population; consult Safety Code 6, obtainable from Health Canada's website www.hc-sc.gc.ca/rpb.

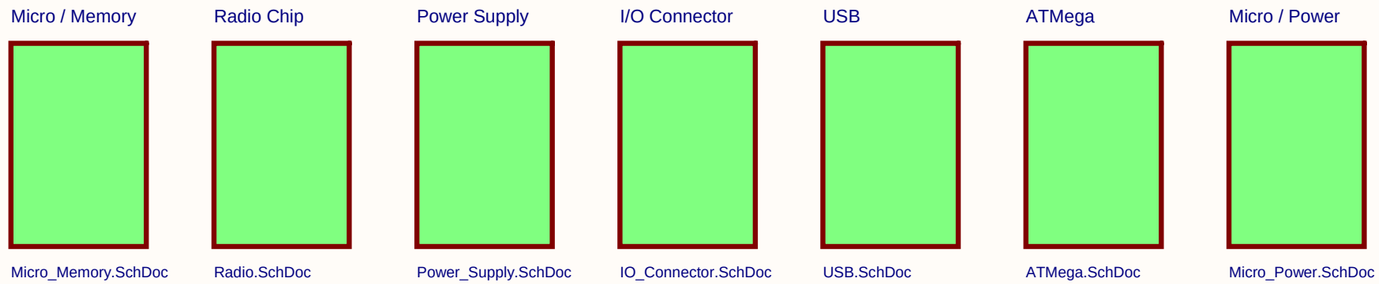
Integrator must place a label outside their product similar to the example show below:

OEM Manufacturer name

Contains transmitter module
FCC ID: UDM3011
UPN: 1894B-3011
Model: 3011

eSPOT

Rev 8.2.2



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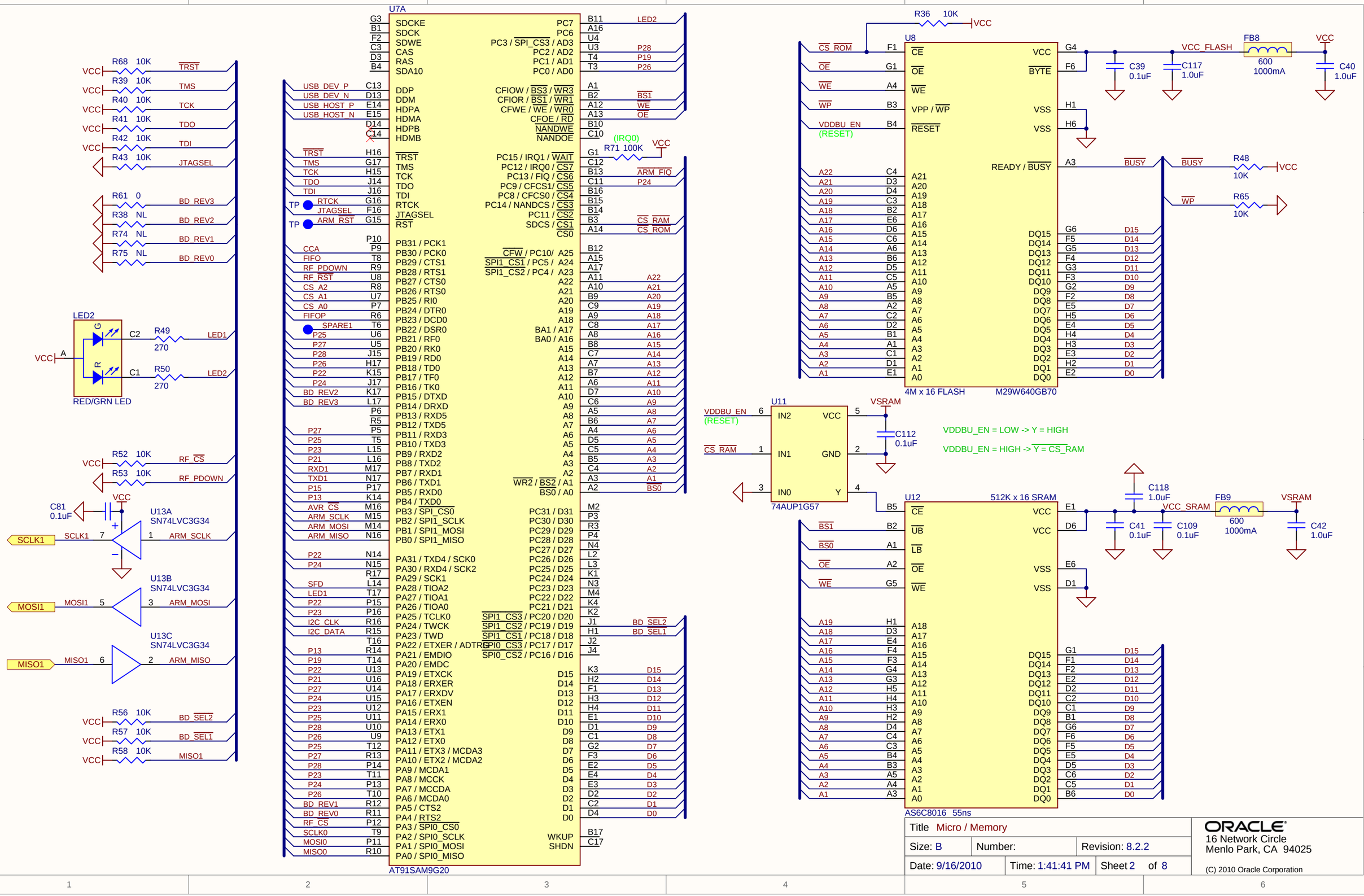
Date: 9/16/2010	Time: 1:41:41 PM	Sheet 1 of 8	

ORACLE
16 Network Circle
Menlo Park, CA 94025


R68 10K VCC TRST
R39 10K VCC TMS
R40 10K VCC TCK
R41 10K VCC TDO
R42 10K VCC TDI
R43 10K JTAGSEL
R61 0 BD_REV3
R38 NL BD_REV2
R74 NL BD_REV1
R75 NL BD_REV0
LED2
VCC A
C2 R49 270 LED1
C1 R50 270 LED2
RED/GRN LED
R52 10K VCC RF_CS
R53 10K VCC RF_PDOWN
C81 0.1uF
VCC
U13A SN74LVC3G34
SCLK1 SCLK1 7 1 ARM_SCLK
U13B SN74LVC3G34
MOSI1 MOSI1 5 3 ARM_MOSI
U13C SN74LVC3G34
MISO1 MISO1 6 2 ARM_MISO
R56 10K VCC BD_SEL2
R57 10K VCC BD_SEL1
R58 10K VCC MISO1
U7A
AT91SAM9G20
USB_DEV_P USB_DEV_N USB_HOST_P USB_HOST_N
TRST TMS TCK TDO TDI
TP RTCK JTAGSEL
TP ARM_RST
CCA FIFO RF_PDOWN RF_RST CS_A2 CS_A1 CS_A0 FIFOP
TP SPARE1
P25 P27 P28 P26 P22 P24 BD_REV2 BD_REV3
P27 P25 P23 P21 RXD1 TXD1 P15 P13 AVR_CS ARM_SCLK ARM_MOSI ARM_MISO
P22 P24 SFD LED1 P22 P23 I2C_CLK I2C_DATA P13 P19 P22 P21 P27 P24 P23 P25 P28 P26 P25 P27 P26 P23 P24 P26 BD_REV1 BD_REV0 RF_CS SCLK0 MOSI0 MISO0
PC7 PC6 PC3 / SPI_CS3 / AD3 PC2 / AD2 PC1 / AD1 PC0 / AD0
CFIOW / BS3 / WR3 CFIOR / BS1 / WR1 CFWE / WE / WR0 CFOE / RD NANDWE NANDOE
PC15 / IRQ1 / WAIT PC12 / IRQ0 / CS7 PC13 / FIQ / CS6 PC9 / CFCS1/ CS5 PC8 / CFCS0 / CS4 PC14 / NANDCS / CS3 PC11 / CS2 SDCS / CS1 CS0
CFW / PC10/ SPI1_CS1 / PC5 / SPI1_CS2 / PC4 /
PB31 / PCK1 PB30 / PCK0 PB29 / CTS1 PB28 / RTS1 PB27 / CTS0 PB26 / RTS0 PB25 / RI0 PB24 / DTR0 PB23 / DCD0 PB22 / DSR0 PB21 / RF0 PB20 / RK0 PB19 / RD0 PB18 / TD0 PB17 / TF0 PB16 / TK0 PB15 / DTXD PB14 / DRXD PB13 / RXD5 PB12 / TXD5 PB11 / RXD3 PB10 / TXD3 PB9 / RXD2 PB8 / TXD2 PB7 / RXD1 PB6 / TXD1 PB5 / RXD0 PB4 / TXD0 PB3 / SPI_CS0 PB2 / SPI1_SCLK PB1 / SPI1_MOSI PB0 / SPI1_MISO
PA31 / TXD4 / SCK0 PA30 / RXD4 / SCK2 PA29 / SCK1 PA28 / TIOA2 PA27 / TIOA1 PA26 / TIOA0 PA25 / TCLK0 PA24 / TWCK PA23 / TWD PA22 / ETXER / ADTRG PA21 / EMDIO PA20 / EMDC PA19 / ETXCK PA18 / ERXER PA17 / ERXDV PA16 / ETXEN PA15 / ERX1 PA14 / ERX0 PA13 / ETX1 PA12 / ETX0 PA11 / ETX3 / MCDA3 PA10 / ETX2 / MCDA2 PA9 / MCDA1 PA8 / MCCK PA7 / MCCDA PA6 / MCDA0 PA5 / CTS2 PA4 / RTS2 PA3 / SPI0_CS0 PA2 / SPI0_SCLK PA1 / SPI0_MOSI PA0 / SPI0_MISO
WR2 / BS2 / A1 BS0 / A0
SPI1_CS3 / PC20 / D20 SPI1_CS2 / PC19 / D19 SPI1_CS1 / PC18 / D18 SPI0_CS3 / PC17 / D17 SPI0_CS2 / PC16 / D16
PC31 / D31 PC30 / D30 PC29 / D29 PC28 / D28 PC27 / D27 PC26 / D26 PC25 / D25 PC24 / D24 PC23 / D23 PC22 / D22 PC21 / D21
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
WKUP SHDN
LED2 P28 P19 P26 (IRQ0) R71 100K VCC ARM_FIQ P24 CS_RAM CS_ROM A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 BS0 BD_SEL2 BD_SEL1 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 B17 C17
R36 10K VCC
U8
CS_ROM OE WE WP VDDBU_EN (RESET)
F1 G1 A4 B3 B4
CE OE WE VPP / WP RESET
VCC BYTE VSS VSS READY / BUSY
G4 F6 H1 H6 A3
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1
C4 D3 D4 C3 B2 E6 D6 C6 A6 B6 D5 C5 A5 B5 A8 A7 B1 A2 C1 D1 E1
A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
G6 F5 G5 F4 G3 F3 G2 E5 H5 E4 H4 E3 H2 E2
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1
4M x 16 FLASH M29W640GB70
C39 0.1uF C117 1.0uF VCC_FLASH FB8 600 1000mA VCC C40 1.0uF
BUSY R48 10K VCC
WP R65 10K
U11
VDDBU_EN (RESET) CS_RAM
6 1
IN2 IN1 IN0 VCC GND Y
5 2 4
3
74AUP1G57
VSRAM C112 0.1uF
VDDBU_EN = LOW -> Y = HIGH
VDDBU_EN = HIGH -> Y = CS_RAM
U12 512K x 16 SRAM
B5 B2 A1 A2 G5
CE UB LB OE WE
VCC VCC VSS VSS
E1 D6 E6 D1
BS1 BS0 OE WE
A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1
H1 D3 E4 F4 F3 G4 G3 H5 H4 H3 H2 D4 C4 C3 B4 B3 A5 A4 A3
A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
G1 F1 F2 E2 D2 C2 C1 B1 G6 F6 C5 D5 E5 D4 C6 B6
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
AS6C8016 55ns
C118 1.0uF C41 0.1uF C109 0.1uF VCC_SRAM FB9 600 1000mA VSRAM C42 1.0uF
Title Micro / Memory
Size: B Number: Revision: 8.2.2
Date: 9/16/2010 Time: 1:41:41 PM Sheet 2 of 8
ORACLE
16 Network Circle
Menlo Park, CA 94025
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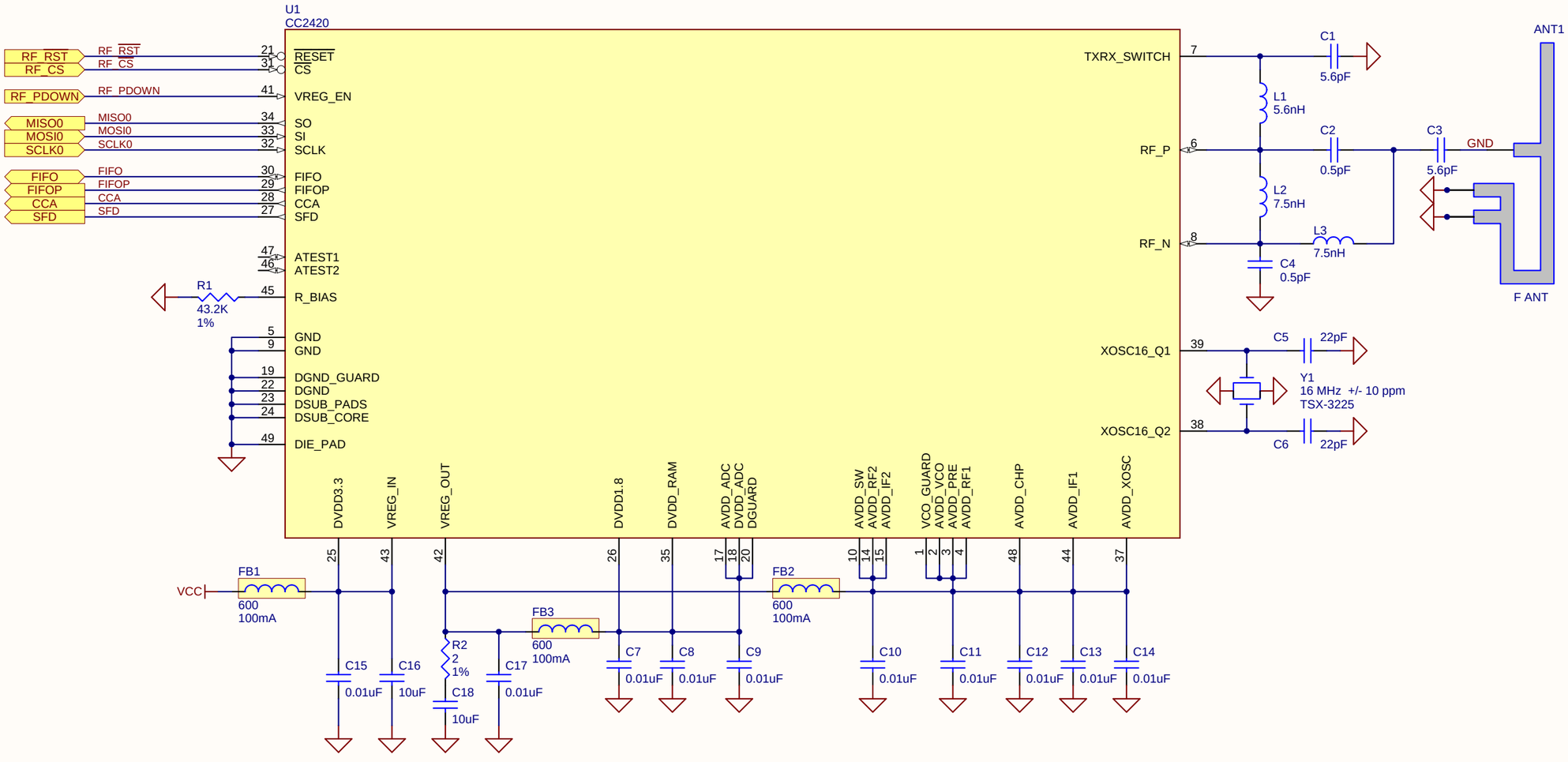
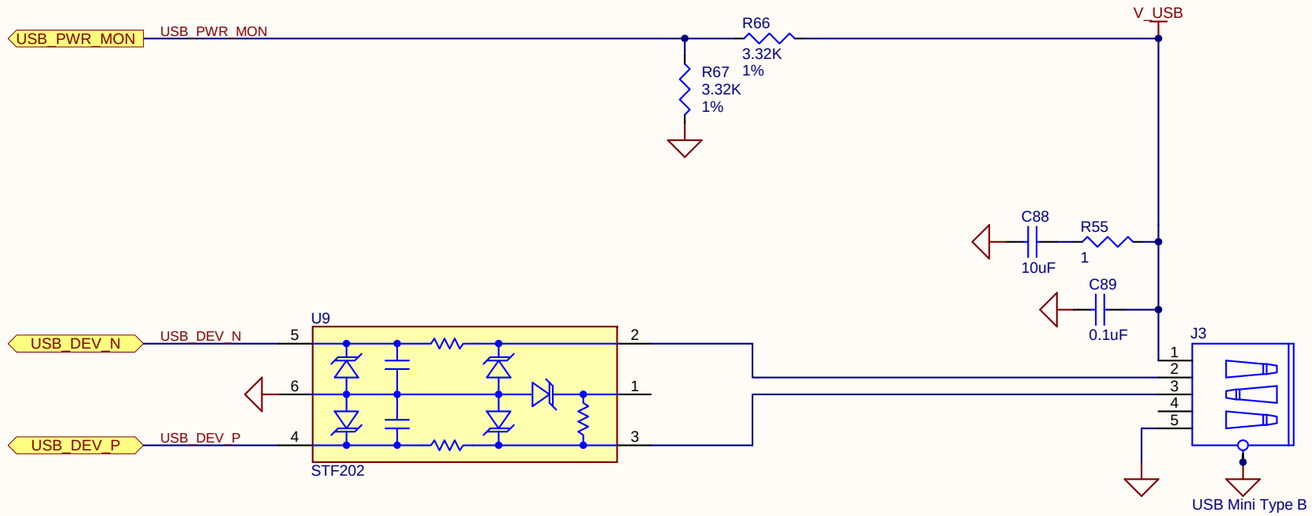
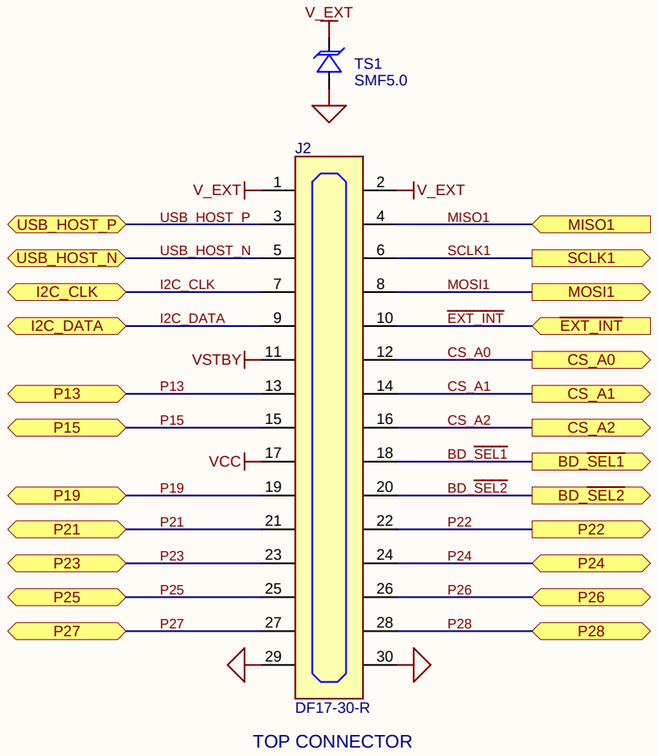


Title Chipcon CC2420 Transceiver			ORACLE 16 Network Circle Menlo Park, CA 94025
Size: B	Number:	Revision: 8.2.2	
Date: 9/16/2010	Time: 1:41:41 PM	Sheet 3 of 8	

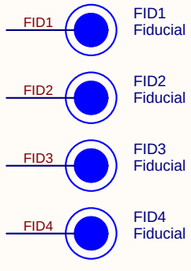


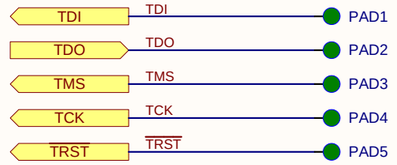
Title USB Device		
Size: B	Number:	Revision: 8.2.2
Date: 9/16/2010	Time: 1:41:41 PM	Sheet 4 of 8

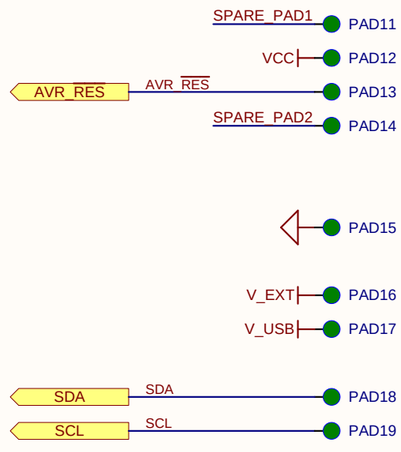
ORACLE
16 Network Circle
Menlo Park, CA 94025



TOP CONNECTOR

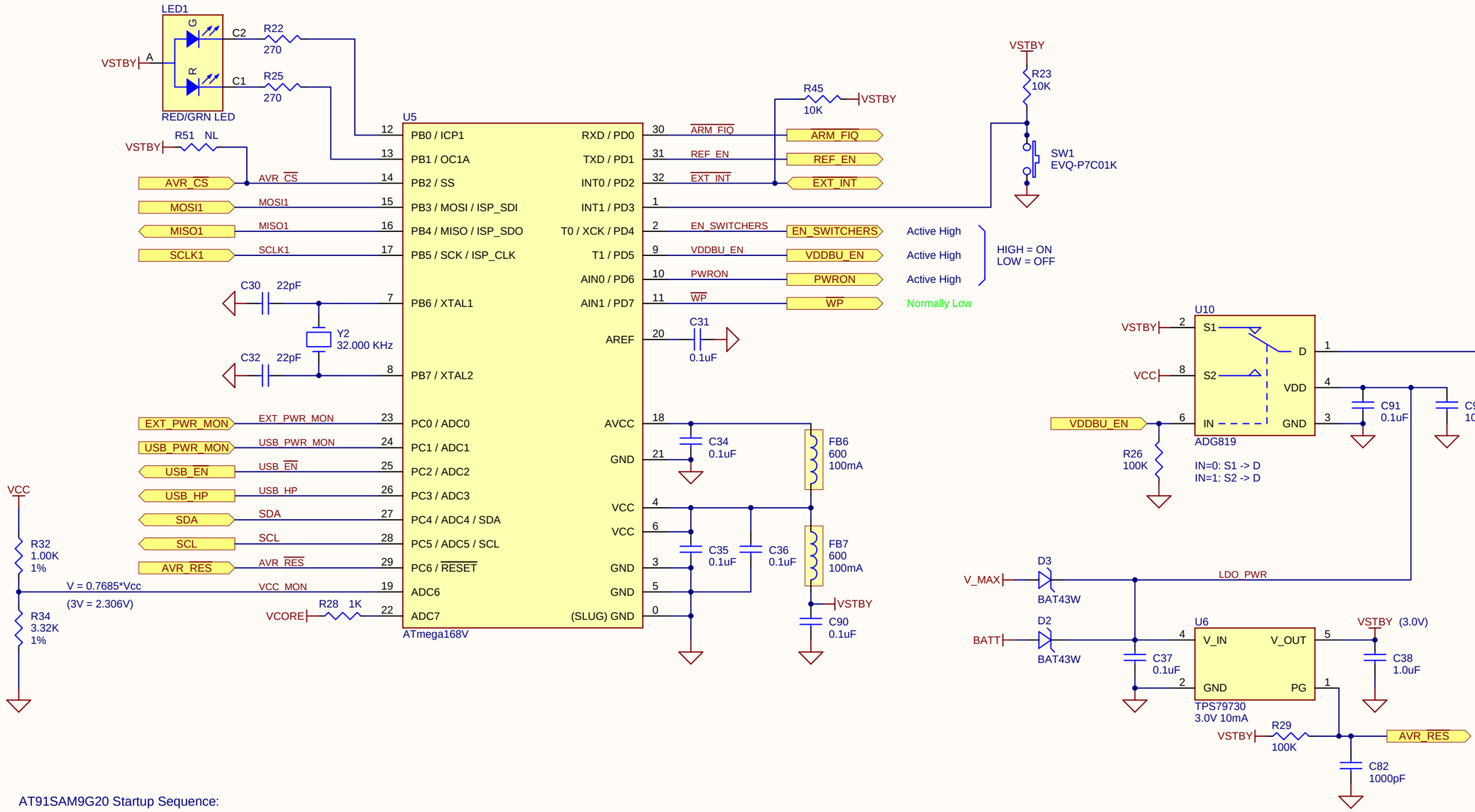






Title USB		
Size: B	Number:	Revision: 8,2.2
Date: 9/16/2010	Time: 1:41:41 PM	Sheet 5 of 8

ORACLE
16 Network Circle
Menlo Park, CA 94025

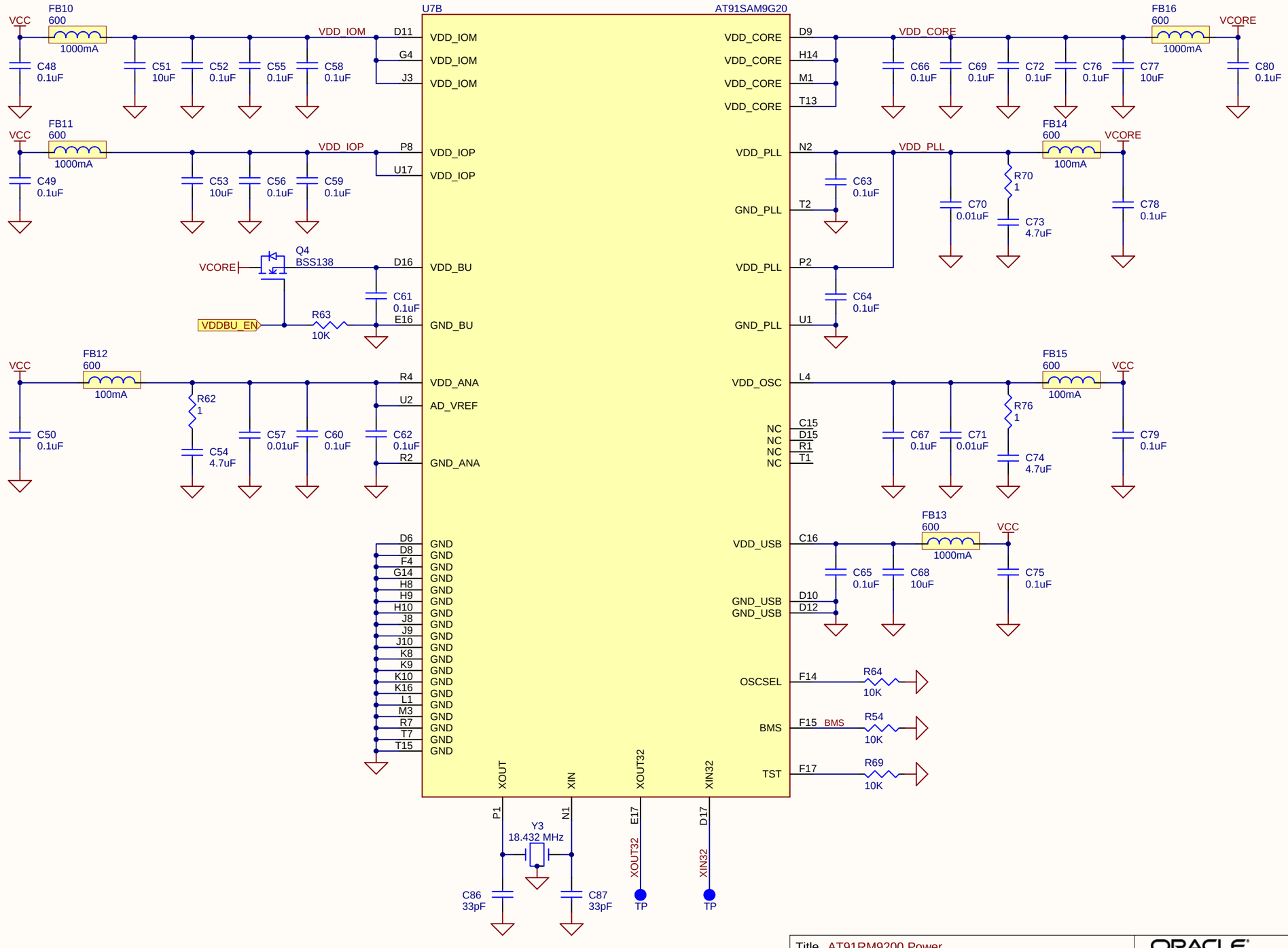


AT91SAM9G20 Startup Sequence:

Set PWRON = High
Set EN_SWITCHERS = High
Wait for 1.0V and 3.0V to stabilize
Set VDDBU_EN = High
Wait 150 us for RC clock to start

Title ATmega		
Size: B	Number:	Revision: 8.2.2
Date: 9/16/2010	Time: 1:41:42 PM	Sheet 6 of 8

ORACLE
16 Network Circle
Menlo Park, CA 94025



Title AT91RM9200 Power			
Size: B	Number:	Revision: 8.2.2	
Date: 9/16/2010	Time: 1:41:42 PM	Sheet 7 of 8	

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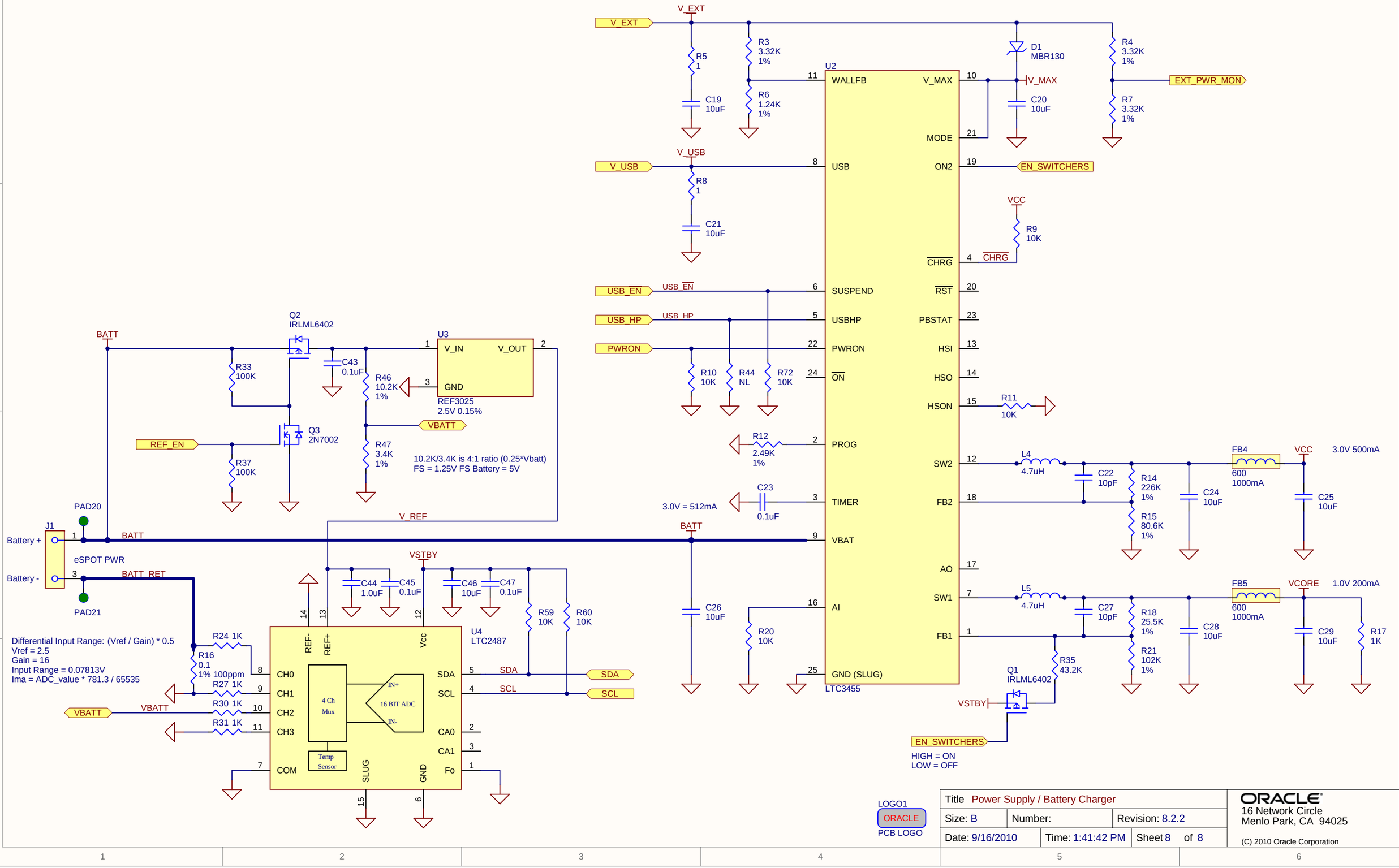
16 Network Circle
Menlo Park, CA 94025


V_EXT
R5
1
C19
10uF
R3
3.32K
1%
R6
1.24K
1%
U2
WALLFB
V_MAX
MODE
D1
MBR130
V_MAX
C20
10uF
R4
3.32K
1%
R7
3.32K
1%
EXT_PWR_MON
V_USB
R8
1
C21
10uF
USB
ON2
EN_SWITCHERS
VCC
R9
10K
CHRG
USB_EN
USB_EN
SUSPEND
RST
USB_HP
USB_HP
USBHP
PBSTAT
PWRON
PWRON
HSI
R10
10K
R44
NL
R72
10K
ON
HSO
HSON
R11
10K
R12
2.49K
1%
PROG
C23
0.1uF
TIMER
3.0V = 512mA
BATT
VBAT
C26
10uF
R20
10K
AI
GND (SLUG)
LTC3455
SW2
L4
4.7uH
C22
10pF
R14
226K
1%
R15
80.6K
1%
C24
10uF
FB4
600
1000mA
VCC
3.0V 500mA
C25
10uF
FB2
AO
SW1
L5
4.7uH
C27
10pF
R18
25.5K
1%
R21
102K
1%
C28
10uF
FB5
600
1000mA
VCORE
1.0V 200mA
C29
10uF
R17
1K
FB1
R35
43.2K
Q1
IRLML6402
VSTBY
EN_SWITCHERS
HIGH = ON
LOW = OFF
BATT
Q2
IRLML6402
R33
100K
C43
0.1uF
R46
10.2K
1%
U3
V_IN
V_OUT
GND
REF3025
2.5V 0.15%
VBATT
Q3
2N7002
REF_EN
R37
100K
R47
3.4K
1%
10.2K/3.4K is 4:1 ratio (0.25*Vbatt)
FS = 1.25V FS Battery = 5V
PAD20
J1
Battery +
Battery -
eSPOT PWR
PAD21
BATT
BATT_RET
V_REF
VSTBY
C44
1.0uF
C45
0.1uF
C46
10uF
C47
0.1uF
R59
10K
R60
10K
U4
LTC2487
REF-
REF+
Vcc
CH0
CH1
CH2
CH3
COM
SLUG
GND
SDA
SCL
CA0
CA1
Fo
4 Ch
Mux
IN+
IN-
16 BIT ADC
Temp
Sensor
SDA
SCL
Differential Input Range: (Vref / Gain) * 0.5
Vref = 2.5
Gain = 16
Input Range = 0.07813V
Ima = ADC_value * 781.3 / 65535
R24 1K
R16
0.1
1% 100ppm
R27 1K
R30 1K
R31 1K
VBATT
LOGO1
ORACLE
PCB LOGO
Title Power Supply / Battery Charger
Size: B
Number:
Revision: 8.2.2
Date: 9/16/2010
Time: 1:41:42 PM
Sheet 8 of 8
ORACLE
16 Network Circle
Menlo Park, CA 94025
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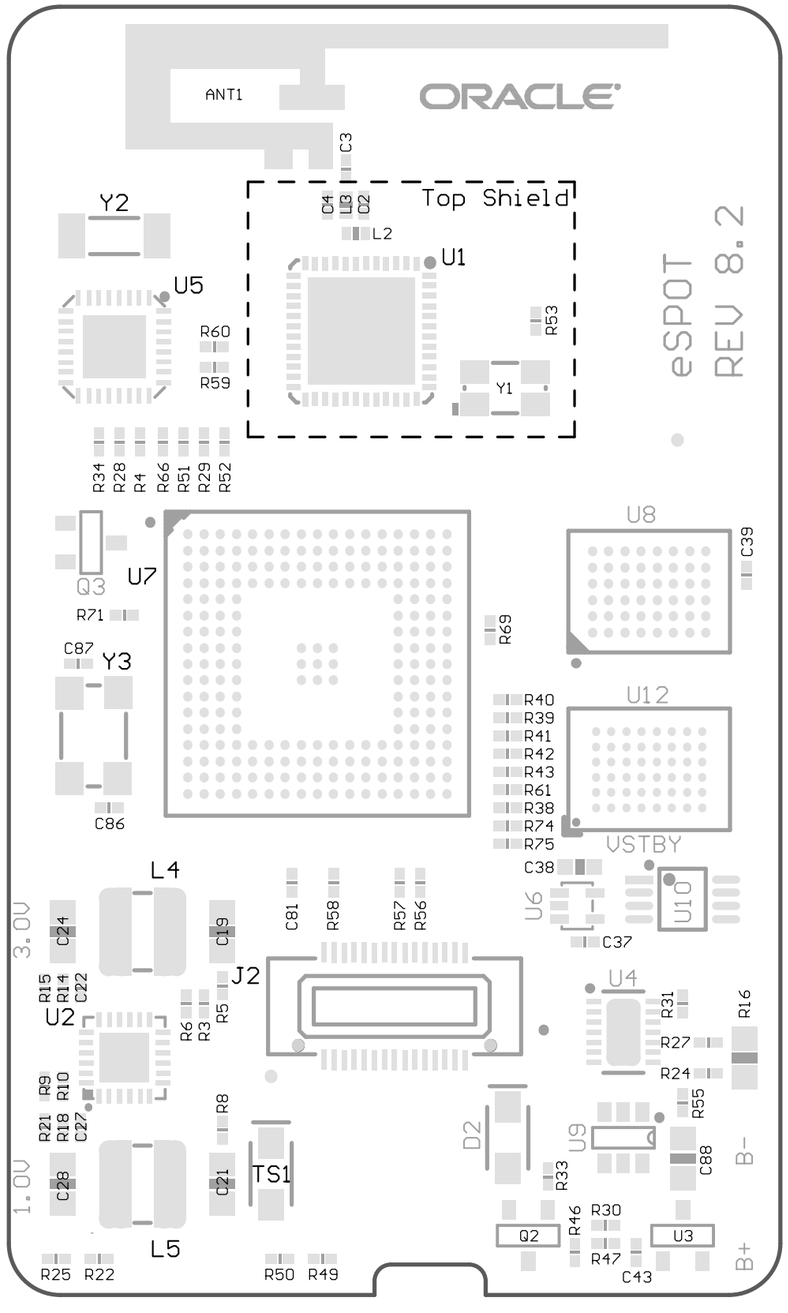
eSPOT
ASSEMBLY TOP
REV 8.2.2

Assembly Notes:

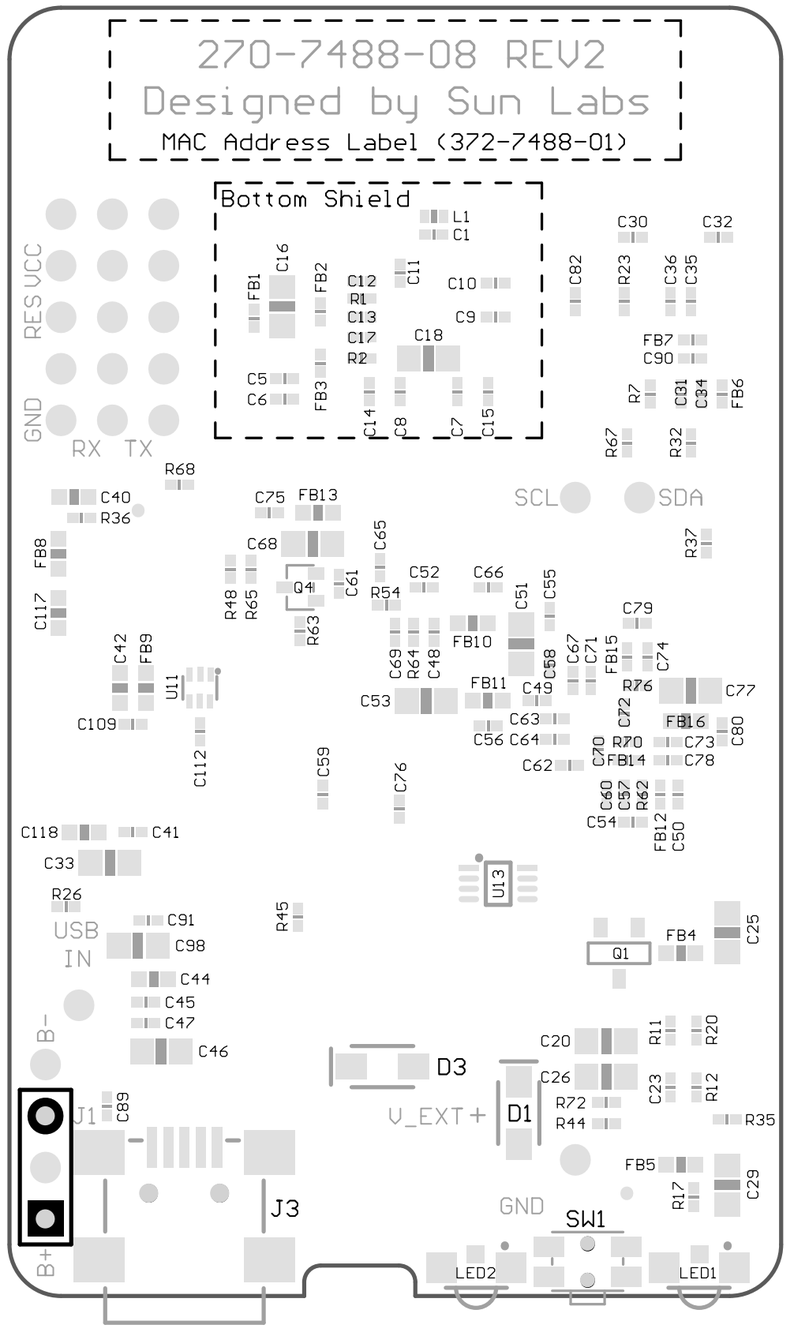
Use RoHS-6 compliant assembly process
(Lead-Free)

Wash board to remove flux
Bake after washing to dry

Label Locations - Top Side:
Top Shield or U7



eSPOT
ASSEMBLY BOTTOM
REV 8.2.2



Do not put QC stamp markings over test-point pads

Label Locations - Bottom Side:
Bottom Shield

MAC Address Label:
- Label material must be non-metalic
- Typical label size: 1.000 x 0.250
- Max label size: 1.100 x 0.275
- Format: 0000.0000